



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Michael Y. Lai

§ Art Unit: 2192

Serial No.: 10/674,364

§ Examiner: Isaac Tuku Tecklu

Filed: September 29, 2003

§ Atty Docket: ITL.1482US  
(P16116)

For: Method and Apparatus for  
Bit Field Optimization

§ Assignee: Intel Corporation

Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**REPLY BRIEF**

In response to the Examiner's Answer, the following Reply Brief is submitted.

It is respectfully submitted that the Examiner's Answer does nothing to advance the issue raised in the appeal brief: "Where does the reference teach modifying the intermediate representation to more efficiently execute the one or more instructions for processing a bit field data?" It is respectfully submitted that the best understanding that can be obtained from the Answer is that the Examiner admits that no such teaching is provided in the reference. Instead, the Examiner relies on M.P.E.P. § 2111.01 for the proposition that he can simply read out of the claim what he claims to be an intended use.

Claim 1 has no intended use. It is a method claim that tells how the intermediate must be modified. It must be modified to more efficiently execute the one or more instructions for

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processing the bit field data. It is not seen how anything in Section 2111.01 has anything to do with claiming an intended use.

To the contrary, there is no proposition that an intended use can be given no weight in the body of the claim. For example, M.P.E.P. § 2111.04 points out that claim scope is not limited by claim language that suggests or makes optional, but does not require steps to be performed. Here, however, claim 1 clearly requires that the intermediate representation be modified in a way to make the execution of the one or more instructions for processing the bit field more efficient. As pointed out in the Manual of Patent Examining Procedure in that section, even a whereby clause "cannot be ignored in order to change the substance of the invention." The case law is clear that language to do something provides a limiting effect. See *In re Venezia*, 530 F.2d 956 (C.C.P.A. 1976) (claim phrases including members adapted to be positioned, "serve to precisely define present structural attributes" [Emphasis added]. To the same effect is M.P.E.P. § 2173.05(g) ("A function limitation must be evaluated and considered just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used.").

Certainly, there is no proposition, contrary to the position taken by the Examiner, that would shift the burden of proof to the applicant to prove that a 158 page reference does not do what is claimed in the face of the Examiner's failure to point out anything within that reference that suggests that it does do what is claimed. The patent prosecution process does not go forward with the Examiner simply citing a big, fat reference and insisting that the applicant prove that the reference does not do what is claimed.

The Answer on page 13, above the heading b, states that "The bit field here has been used to facilitate execution and/or control of such a CALL routine instruction efficiently when the bit field is True and when it is False." But, even if this is true, this is the opposite of what is claimed. It is not the bit field that facilitates execution, but, instead, it is the intermediate representation that is modified to more efficiently execute one or more instructions for processing the bit field. Thus, it is respectfully submitted that the Examiner simply has not addressed the claimed limitation, for the reasons described above, that the pertinent limitations have been read out of the claim.

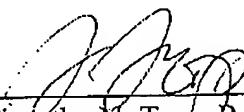
Similarly, it is not disputed that there is modification of the intermediate representation in the cited reference. The issue, as set forth in the Appeal Brief, was whether the reference teaches

modification of the intermediate representation "to more efficiently execute the one or more instructions for processing the bit field data." It appears that the Examiner acknowledges that it does not.

The suggestion on page 14 of the Examiner's Answer that the appellant is arguing that Ty modifies the instructions to be less efficient is simply unwarranted. No such argument was ever made. It is not material to the limitation of the claim as to whether or not, in general, the modification of the intermediate instructions makes execution of some intermediate instructions more or less efficient. The question is whether or not the modification of the intermediate instructions somehow makes more efficient the execution of the bit field. All the Examiner has done is to identify data which the Examiner contends corresponds to the bit field. He has not and cannot identify any instructions that are modified to more efficiently execute the one or more instructions for processing the bit field data. Instead, he argues, on page 13 before the heading b, that the bit field is used to facilitate instruction and/or control of the CALL routine instruction efficiently. But this is not what is claimed. There is no showing that any instructions for executing the bit field are modified in some way to make those instructions more efficient executors of the bit field data.

Therefore, the rejection should be reversed.

Respectfully submitted,



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